1763

PATENT
(5298-04700/PM00028)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No. 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A PLANARIZED SEMICONDUCTOR STRUCTURE

§ Group Art Unit: 1763
§ Examiner: Goudreau, G.
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§ Atty. Dkt. No. 5298-04700
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I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: **Box Non-Fee Amendment,** Assistant Commissioner for Patents, Washington, D.C. 20231, on the date indicated below:

November 19, 2002
Date

Kevin L. Daffer

AMENDMENT; RESPONSE TO OFFICE ACTION MAILED JULY 25, 2002

Box: Non-Fee Amendment
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This paper is submitted in response to the Office Action mailed July 25, 2002 to further highlight reasons why the application is in condition for allowance.

Please amend the case as follows.

IN THE SPECIFICATION

Please replace pg. 23, line 11 - pg. 24, line 3, with the amended paragraph below. A "marked-up" version of each amendment is included in **Attachment A**.

In an alternative embodiment, the polishing process may be designed to terminate at an elevation within intermediate layer 33. As such, the polishing process may terminate above or within intermediate layer 33, including above or within dielectric 32 and/or layer 34. In this manner, the polishing of underlying layer 42 may be substantially terminated upon exposing layer 34 or dielectric 32.